CLAIMS

What is claimed is:

1. A non-volatile memory circuit comprising:

a first inverter which comprises a first transistor and a second transistor each having a gate and a drain, the gates of said first and second transistors being connected to each other, and the drains of said first and second transistors being connected to each other with a first node therebetween;

a second inverter which comprises a third transistor and a fourth transistor each having a gate and a drain, the gates of said third and fourth transistors being connected to each other, and the drains of said third and fourth transistors being connected to each other with a second node therebetween;

a fifth transistor which comprises a gate and is connected between a first bit line and said first node, said gate being connected to a word line; and

a sixth transistor which comprises a gate and is connected between a second bit line and said second node, the gate being connected to said word line;

said first node being connected to the gate of said third transistor and to the gate of said fourth transistor;

said second node being connected to the gate of said first transistor and to the gate of said second transistor;

the source of said first transistor and the source of said third transistor being connected to a ground line;

the source of said second transistor and the source of said fourth transistor being connected to a power line;

the circuit further being provided with a first resistor element and a second resistor element whose resistance values can be electrically modified;

the positional relationship of said first resistor element and said second resistor element being selected from the following first to fourth positional relationships:

a first positional relationship in which said first resistor element is connected between the source of said first transistor and said ground line, and said second resistor element is connected between the source of said third transistor and said ground line;

a second positional relationship in which said first resistor element is connected between the source of said second transistor and said power line, and said second resistor element is connected between the source of said fourth transistor and said power line;

a third positional relationship in which said first resistor element is connected between said first node and the drain of said first transistor, and said second resistor element is connected between said second node and the drain of said third transistor; and

a fourth positional relationship in which said first resistor element is connected between said first node and the drain of said second transistor, and said second resistor element is connected between said second node and the drain of said fourth transistor.

2. A non-volatile memory circuit according to claim 1, in which the positional relationship is said first positional relationship.

3. A non-volatile memory circuit according to claim 1, in which the positional relationship is said second positional relationship.

4. A non-volatile memory circuit according to claim 1, in which said positional relationship is the third positional relationship.

5. A non-volatile memory circuit according to claim 1, in which the positional relationship is said fourth positional relationship.

6. A non-volatile memory circuit according to claim 1, in which the positional relationship is said first positional relationship;

the circuit further comprising a third transistor element and a fourth transistor element;

said third resistor element being connected between the source of said second transistor and said power line, and said fourth resistor element being connected between the source of said fourth transistor and said power line.

7. A non-volatile memory circuit according to claim 1, in which said first and third transistors are N-type transistors; and

said second and fourth transistors are P-type transistors.

8. A non-volatile memory circuit according to claim 1, in which said first and second transistors are both N- or both P-type transistors and have different threshold voltage values; and

said third and fourth transistors are both N- or both P-type transistors and have different threshold voltage values.

9. A non-volatile memory circuit according to claim 1, in which said first and second resistor elements comprise a material whose resistance value can be changed by heat generated by an electric current.

10. A non-volatile memory circuit according to claim 9, in which said first and second resistor elements comprise a chalcogenide-based phase-change material or a perovskite-type strongly correlated electron material.

11. A non-volatile memory circuit according to claim 1, in which said first and second resistor elements comprise a magnetic material whose resistance value can be changed by the application of a magnetic field;

the circuit further comprising a first magnetic field control line which can alter the direction of magnetization of the magnetic material in said first resistor element and a second magnetic field control line which can alter the direction of magnetization of the magnetic material in said second resistor element.

12. A non-volatile memory circuit according to claim 1, in which said first and second resistor elements comprise a material whose resistance value can be changed by the TMR effect or the GMR effect.

13. A method for driving a non-volatile memory circuit comprising:

a first inverter which comprises a first transistor and a second transistor each having a gate and a drain, the gates of said first and second transistors being connected to each other, and the drains of said first and second transistors being connected to each other with a first node therebetween;

a second inverter which comprises a third transistor and a fourth transistor each having a gate and a drain, the gates of said third and fourth transistors being connected to each other, and the drains of said third and fourth transistors being connected to each other with a second node therebetween;

a fifth transistor which comprises a gate and is connected between a first bit line and said first node, said gate being connected to a word line; and

a sixth transistor which comprises a gate and is connected between a second bit line and said second node, said gate being connected to said word line;

said first node being connected to the gate of said third transistor and to the gate of said fourth transistor;

said second node being connected to the gate of said first transistor and to the gate of said second transistor;

the source of said first transistor and the source of said third transistor being connected to a ground line;

the source of said second transistor and the source of said fourth transistor being connected to a power line;

the circuit further being provided with a first resistor element and a second resistor element whose resistance values can be electrically modified;

the positional relationship of said first resistor element and said second resistor element being selected from the following first to fourth positional relationships:

a first positional relationship in which said first resistor element is connected between the source of said first transistor and said ground line, and said second resistor element is connected between the source of said third transistor and said ground line;

a second positional relationship in which said first resistor element is connected between the source of said second transistor and said power line, and said second resistor element is connected between the source of said fourth transistor and said power line;

a third positional relationship in which said first resistor element is connected between said first node and the drain of said first transistor, and said second resistor element is connected between said second node and the drain of said third transistor; and

a fourth positional relationship in which said first resistor element is connected between said first node and the drain of said second transistor, and said second resistor element is connected between said second node and the drain of said fourth transistor;

the method comprising:

a STORE step including a first step wherein the resistance values of said first and second resistor elements are reduced to low levels before power to said non-volatile memory circuit is removed; and a second step, which follows said first step, wherein the resistance value of one of said first and second resistor elements is increased to a high level; and

a RECALL step wherein voltages are applied to said word line, said first and second bit lines and said power line at a predetermined time after power supply to said non-volatile memory circuit is started.

14. A method for driving the non-volatile memory circuit according to claim 13, in which said RECALL step comprises a step wherein said word line is set at a high voltage level, and the voltages applied to said power line, said first bit line and said second bit line are slowly increased to the supply voltage level.

15. A method for driving the non-volatile memory circuit according to claim 13, in which said RECALL step comprises a step wherein predetermined voltages are applied to said first and second bit lines, and, in this state, said word line is set to a high voltage level, and the voltage applied to said power line is slowly increased to the supply voltage level.

16. A method for driving the non-volatile memory circuit according to claim 13, in which said RECALL step comprises a step wherein predetermined voltages are applied to said first and second bit lines, and, in this state, the voltage applied to the word line is slowly increased to a high level, and the voltage applied to said power line is slowly increased to the supply voltage level.

17. A method for driving the non-volatile memory circuit according to claim 13, in which the positional relationship is either of said first positional relationship or said third positional relationship;

said first and second resistor elements comprising a material whose resistance value can be changed by heat generated by an electric current;

the first step further comprising a third step wherein a supply voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and the voltage of said word line is changed from a high level to a low level after a first period; and

the second step further comprising a fourth step wherein the supply voltage is applied to said first bit line, a voltage lower than the supply voltage is applied to said second bit line, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a second period.

18. A method for driving the non-volatile memory circuit according to claim 13, in which the positional relationship is either said second positional relationship or said fourth positional relationship;

said first and second resistor elements comprising a material whose resistance value can be changed by heat generated by an electric current;

the first step comprising a third step wherein a ground voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a first period; and

the second step comprising a fourth step wherein the ground voltage is applied to said first bit line, a voltage higher than the ground voltage is applied to said second bit line, and, in this state, the voltage of said word line is changed from a high level to a low level, and then the voltage of said word line is changed from a high level to a low level after a second period.

19. A method for driving the non-volatile memory circuit according to claim 13, in which the positional relationship is said first positional relationship;

the circuit further comprising a third resistor element and a fourth resistor element;

said third resistor element being connected between the source of said second transistor and said power line, and said fourth resistor element being connected between the source of said fourth transistor and said power line;

said first to fourth resistor elements comprising a material whose resistance value can be changed by heat generated by an electric current;

the first step comprising:

a third step wherein a supply voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a first period; and

a fourth step wherein the ground voltage is applied to said first and second bit lines, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a second period;

the second step comprising:

a fifth step wherein the supply voltage is applied to said second bit line, a voltage lower than the supply voltage is applied to said first bit line, and, in this state, the voltage of said word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a third period; and

a sixth step wherein the ground voltage is applied to said first bit line, a voltage higher than the ground voltage is applied to said second bit line, and, in this state, the voltage of the word line is changed from a low level to a high level, and then the voltage of said word line is changed from a high level to a low level after a fourth period.

20. A semiconductor device using the non-volatile memory circuit of claim 1 as a memory for storing parameters of a look-up table.

21. A semiconductor device using the non-volatile memory circuit of claim 1 as a memory for controlling circuit interconnection information.

22. A semiconductor device for encryption comprising the non-volatile memory circuit of claim 1.